AN X-BAND HIGH-EFFICIENCY ION-IMPLANTED MMIC POWER AMPLIFIER

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I. ABSTRACT

A state-of-the-art X-band high efficiency monolithic power amplifier has been demonstrated. An average output power of 3.6 Watts at an average 41% power-added efficiency over a 40% bandwidth from 7.0 to 10.5 GHz has been achieved. An excellent average power density of 500 mW/mm and peak power density of 550 mW/mm has been measured across this bandwidth.

II. INTRODUCTION

High-efficiency power amplifiers are key elements in the construction of airborne active array radar systems. X-band MMIC power amplifiers reported before 1985 produced 2 watts of output power with 20% power-added efficiency for about 10% bandwidth using ion implantation technology. Many refinements have been successfully implemented since that time. In 1988, Texas Instruments reported a MMIC chip with 3 watts and 22% efficiency over a 20% bandwidth [1]. In 1989, Avantek reported a partially MMIC chip with 2.5 Watts of output power at 35% efficiency for a 20% bandwidth [2]. This chip was fabricated using molecular beam epitaxy (MBE) grown epitaxial materials and required an off-chip output matching circuit. In 1990, Raytheon produced a 3.7 watt chip at 18% efficiency over a 45% bandwidth [3]. Also in 1990, Hughes Aircraft Company produced a MMIC chip of 1.9 watts at 37% efficiency over a 40% bandwidth with output and input return losses of better than 15 dB [4].

In this paper, we will present the design and performance of a high efficiency MMIC amplifier. Peak output power of 4.0 watts with efficiency of 45% at 8, 8.5 and 10.0 GHz has been obtained at 8 Volts drain bias. Peak efficiencies of about 55% at about 3.2 watts of output power have been measured at 6 volts drain bias.

III. AMPLIFIER DESIGN

Circuit topology, devices selections and models.

A single-ended power amplifier with two stages cascaded has been chosen to provide a minimum power gain of 10 dB. To produce a minimum output power of 33 dBm, 4 power FETs of 1820 μm gate periphery each are stacked in parallel at the output stage. The first stage consists of two power FETs of 1190 μm gate periphery each. In order to improve efficiency, the ratio of the total gate periphery between the driver stage and the output stage is 1 to 3. All of the FETs have a 0.5 μm gate length. The circuit topology is shown in Figure 1.

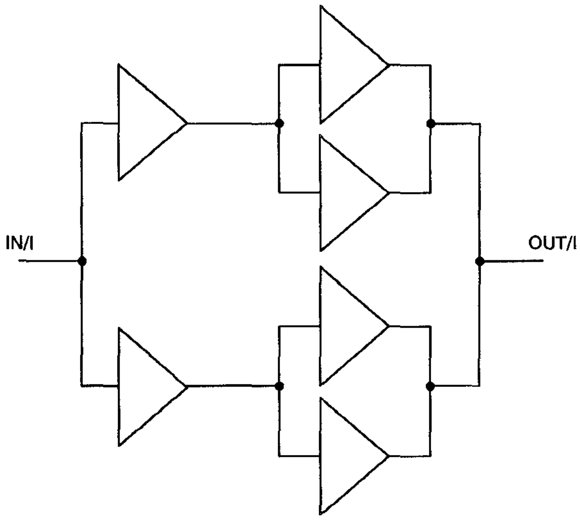

Figure 1 Topology of the amplifier.

The nonlinear models of the FETs are used to generate optimum load impedances presented to the FETs in each stage. The selected devices first are measured at a large matrix of different bias voltages. The three most nonlinear parameters C_{gs} (V_g, V_d), G_m (V_g, V_d), R_o (V_g, V_d) of the driver FETs and the output FETs then are extracted using an in-house program [5],[6]. The optimum load impedances of the FETs at the passband then are generated using the in-house Waveform-Balance program [7]. The detailed procedure is described in reference [4].

Matching networks optimization.

The output matching networks are synthesized and optimized so that optimum load impedances are presented to the output FETs. The interstage matching networks are synthesized and optimized so that optimimum load impedances are presented to the driver FETs. Very careful design of the interstage matching network is required to insure that the driver stage does not saturate before the output stage. Next, the input matching networks are synthesized and optimized for high gain and gain flatness in the passband. The amplifier small signal performance is simulated using Super Compact [8]. The resulting amplifier schematic is shown in Figure 2.

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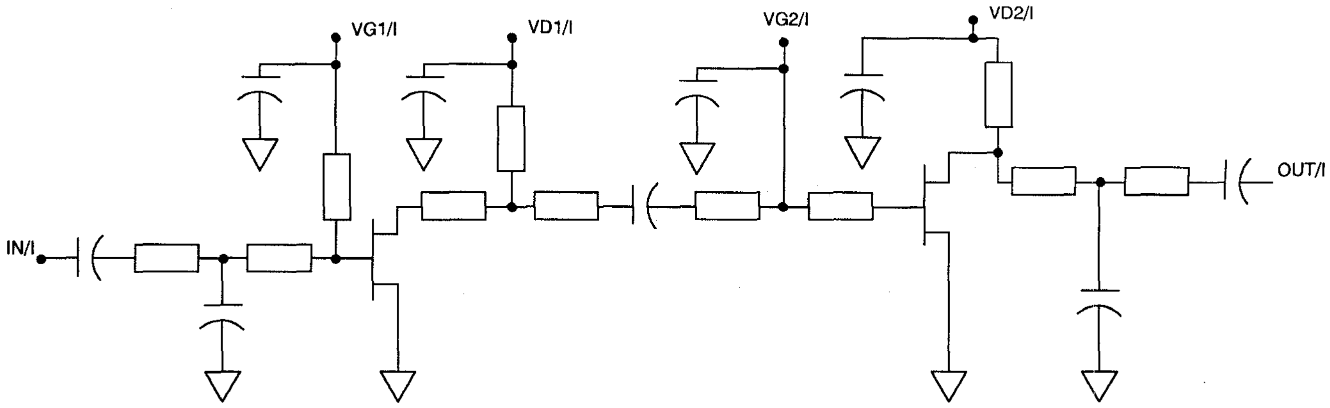

Figure 2 Amplifier schematic.

IV. FABRICATION

The amplifiers are fabricated on a 4-mil substrate using the Hughes standard ion implantation process for MMIC power amplifiers. The block diagram shown in Figure 2 indicates the key features of the process. The four important factors in our process are as follows:

1. The most important factor is the use of ion implantation to optimize the doping profile and the gate recess etch depth [9]. For our application, a double-peak profile with current density about 270 mA/mm of gate periphery provides the best result.
2. Rapid thermal alloy techniques combined with the optimum N+ doping concentration and ohmic metal thickness are used to reduce the ohmic contact resistance which is crucial for the performance of power devices. Ohmic contact resistance of about 0.1 Ω-mm and low knee voltage of about 1 volt have been achieved using this techniques.
3. A self-limiting reactive ion etching [10] is used to etch very small via holes without increasing the dimension of the FET. This is also critical for device uniformity and eventually amplifier yield.
4. Very thick Au metal is applied in the circuit transmission lines to reduce the insertion loss and to improve the current handling capability of the transmission lines for DC biasing. Our transmission lines are 6 μm thick, 3 μm evaporated gold and 3 μm electroplated gold. The chip size is 4.0 by 3.2 mm and the fabricated amplifier is shown in Figure 3.

V. MEASURED PERFORMANCE

We diced the wafer and mounted the amplifier on an ICM test fixture. The measured small signal gain is about 14 to 16 dB within the passband as shown in Figure 4. For power performances, the amplifier is biased at 8 volts at the drain. As shown in Figure 5, the minimum CW output power in this case is 3 watts at 36% efficiency at 10.5 GHz and the maximum CW output power is 4 watts at 45% efficiency at 8.5 to 9.0 GHz. For high efficiency applications, the amplifier is biased at 6 volts at the drain. As shown in Figure 6, the minimum CW output power is 2.2 watts at 38% power-added efficiency at 10.5 GHz and the maximum CW output power is 3.2 watts at 52% efficiency from 7.0 to 9.0 GHz. In either case, the minimum power gain exceeds 10 dB and the minimum output power exceeds 2.2 Watts. The maximum power density is 550 mW/mm at 8.5 and 9.0 GHz. The average power density is 500 mW/mm.

VI. CONCLUSION

High efficiency monolithic power amplifiers have been designed and fabricated using ion-implantation MESFET technology. Peak powers of 4 watts at 7, 8.5 and 9 GHz were obtained at 8 volts drain bias. Peak efficiencies of 56% at 7 GHz and above 50% from 7.5 to 9 GHz were achieved when the drain is biased at 6 volts. In additional, an impressive bandwidth of 40% has been accomplished for both high power and high efficiency cases.

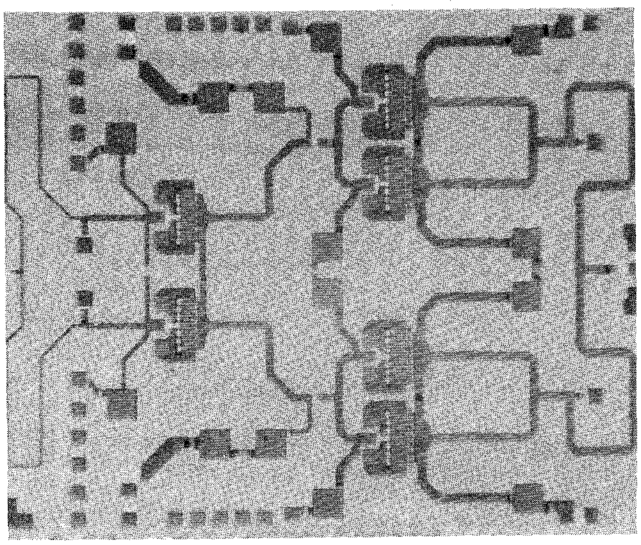

Figure 3 X-band high-efficiency ion-implanted MMIC power amplifier.

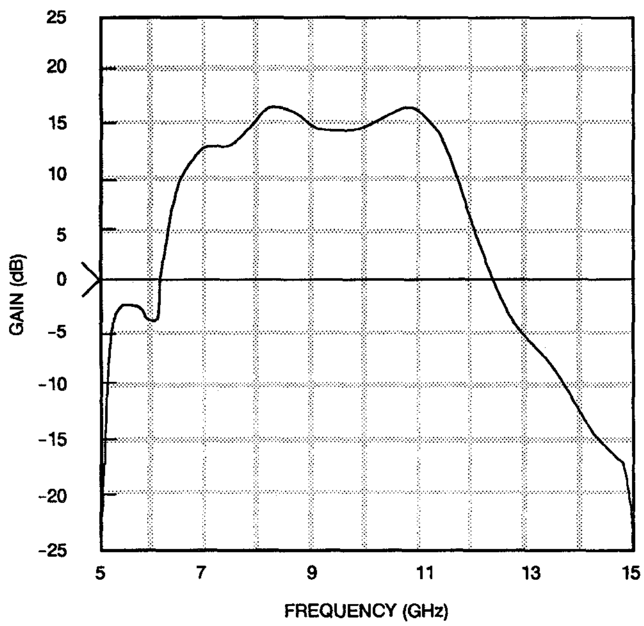

Figure 4 Small signal gain.

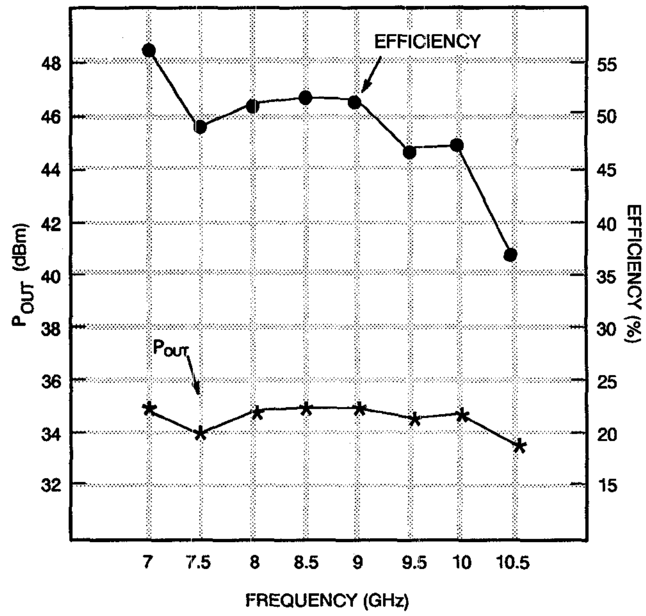

Figure 6 P_{OUT} and efficiency versus frequency.

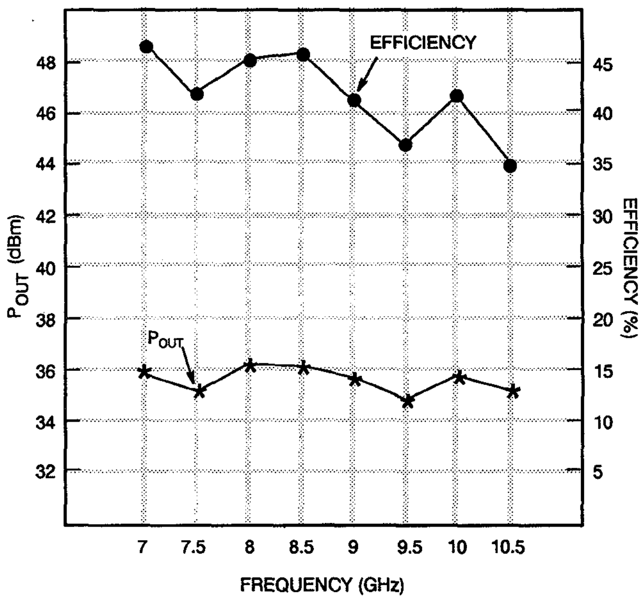

Figure 5 P_{OUT} and efficiency versus frequency.

VII. REFERENCES

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